Automotive Electronics Council
Component Technical Committee

ATTACHMENT 3

AEC - Q100-003 REV-E

MACHINE MODEL ELECTROSTATIC DISCHARGE TEST

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Counsel would especially like to recognize the following significant contributors to the development of this document:

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Automotive Electronics Council
Component Technical Committee

Change Notification

The following summary details the changes incorporated into AEC-Q100-003 Rev-E:

? Section 5, Acceptance Criteria: Added wording to reflect device classification, rather than meeting a 200 volt level.

? Table 3, Integrated Circuit MM ESD Classification Levels: Added new table listing classification levels for MM ESD.

Automotive Electronics Council
Component Technical Committee

METHOD - 003

MACHINE MODEL (MM)
ELECTROSTATIC DISCHARGE (ESD) TEST

Text enhancements and differences made since the last revision of this document are shown as underlined areas.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the MM ESD sensitivity for electronic devices.

1.2 Reference Documents

EOS/ESD Association Specification S5.2
JEDEC Specification EIA/JESD22-A115

1.3 Terms and Definitions

The terms used in this specification are defined as follows.

1.3.1 Device Failure

A condition in which a device does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.2 DUT

An electronic device being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD)

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity

An ESD voltage level resulting in device failure.

DaimlerChrysler	Date	Delphi Delco Electronics Systems	Date	Visteon Corporation	Date
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1.3.5 ESD Simulator

An instrument that simulates the machine model ESD pulse as defined in this specification.

1.3.6 Machine Model (MM) ESD

An ESD pulse meeting the waveform criteria specified in this test method, approximating an ESD pulse from a machine or mechanical equipment.

1.3.7 Major Pulse Period (tpm)

The time (tpm) measured between first and third zero crossing points.

1.3.8 Non-Supply Pins

All pins including, but not limited to, input, output, bi-directional, Vref, Vpp, clock, and “ no-conn pins. These pins do not supply voltage and/or current to the device under test.

1.3.9 Power Pins

All power supply, external voltage source and ground pins. All power pins that are metallically connected together on the chip or in the package shall be treated as one (1) power pin.

1.3.10 PUT

The pin under test.

1.3.11 Withstanding Voltage

The ESD voltage level at which, and below, the device is determined to pass the failure criteria requirements specified in section 4.

1.3.12 Worst-Case Pin Pair (WCP)

WCP is the pin pair representing the worst-case waveform that is within the limits and closest to the minimum or maximum parameter values as specified in Table 1. The WCP shall be identified for each socket. It is permissible to use the worst-case pin pair that has been previously identified by the HBM ESD method (AEC-Q100-002) when performing the Simulator Waveform Verification as defined in section 2.4.

2. EQUIPMENT

2.1 Test Apparatus

The apparatus for this test consists of an ESD pulse simulator and DUT socket. Figure 1 shows a typical equivalent MM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses which meet the waveform requirements of Table 1, Figure 2, and Figure 3.

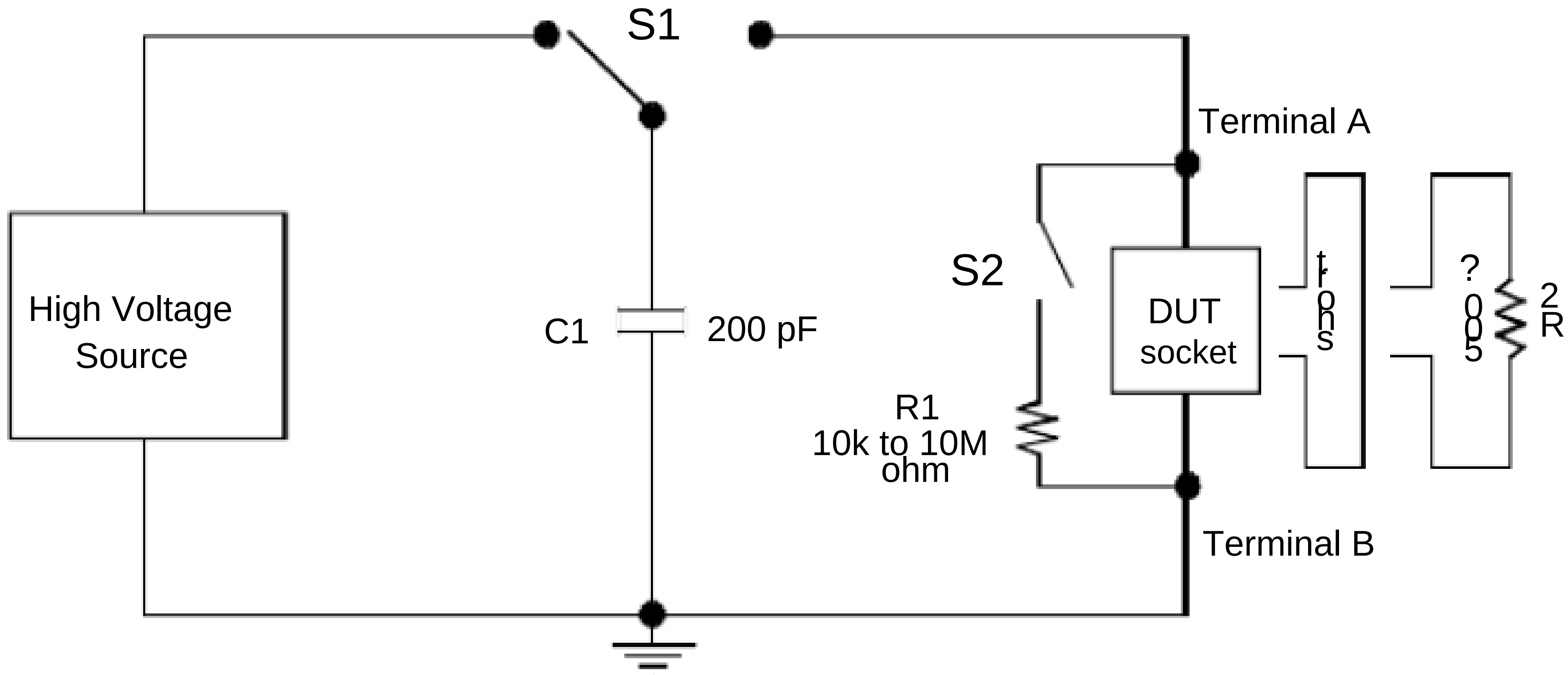

Figure 1: Typical Equivalent MM ESD Circuit

Notes:

1. Figure 1 is shown for guidance only; it does not attempt to represent all associated circuit components, parasitics, etc..
2. The performance of any simulator is influenced by its parasitic capacitance and inductance.
3. Resistor R1, in series with switch S2, ensures a slow discharge of the device.
4. Precautions must be taken in simulator design to avoid recharge transients and multiple pulses.
5. R2, used for Equipment Qualification as specified in section 2.3, shall be a low inductance, 1000 volt, 500 ohm resistor with $\pm$1% tolerance.
6. Piggybacking of DUT sockets (the insertion of secondary sockets into the main DUT socket) is allowed only if the combined piggyback set (main DUT socket with the secondary DUT socket inserted) waveform meets the requirements of Table 1, Figure 2, and Figure 3.
7. Reversal of terminals A and B to achieve dual polarity is not permitted
8. S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

2.2 Measurement Equipment

Equipment shall include an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 1, Figure 2, and Figure 3.

2.2.1 Current Probe

The current probe shall have a minimum bandwidth of 350 MHz and maximum cable length of 1 meter (Tektronix CT-1, CT-2, or equivalent). A CT-2 probe or equivalent should be used with voltages greater than 800 volts.

2.2.2 Evaluation Loads

The two evaluation loads shall be: 1) a low inductance, 1000 volt, 500 ohm sputtered film resistor with ± 1% tolerance, and 2) an 18 AWG tinned copper shorting wire. The lead length of both the shorting wire and the 500 ohm resistor shall be as short as possible and shall span the maximum distance between the worst-case pin pair (WCP) while passing through the current probe as defined in section 2.2.1.

2.2.3 Oscilloscope

The oscilloscope and amplifier combination shall have a minimum bandwidth of 350 MHz, a minimum sensitivity of 100 milliamperes per large division and a minimum visual writing speed of 4 cm per nanosecond.

2.3 Equipment Qualification

Equipment qualification must be performed during initial acceptance testing or after repairs are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 1 and Figure 2 for five (5) consecutive waveforms at all voltage levels using the worst-case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the shorting wire per Figure 1. The simulator must also meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at the 400 volt level using the worst-case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the 500 ohm load per Figure 1. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Simulator Waveform Verification

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified on the worst-case pin pair (WCP) using the shorting wire per section 2.4.1. The worst-case pin pair (WCP) for each socket and DUT board shall be identified and documented. The waveform verification shall be performed when a socket/mother board is changed or on a weekly basis (if the equipment is used for at least 20 hours). If at any time the waveforms do not meet the requirements of Table 1 and Figure 2 at the 400 volt level, the testing shall be halted until waveforms are in compliance.

2.4.1 Waveform Verification Procedure

a. With the required DUT socket installed and with no device in the socket, attach a shorting wire in the DUT socket such that the worst-case pin pair (WCP) is connected between terminal A and terminal B as shown in Figure 1. Place the current probe around the shorting wire.

b. Set the horizontal time scale of the oscilloscope at 20 nanoseconds per division or greater.

c. Initiate a positive pulse at the 400 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

d. Measure and record the first peak current, second peak current, and major pulse period. All parameters must meet the limits specified in Table 1 and Figure 2.

e. Initiate a negative pulse at the 400 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

f. Measure and record the first peak current, second peak current, and major pulse period. All parameters must meet the limits specified in Table 1 and Figure 2.

Table 1: MM Waveform Specification

Voltage Level (V)	Positive First Peak Current for Short, I_{ps1} (A)	Positive Second Peak Current for Short, I_{ps2} (A)	Major Pulse Period for Short, t_{pm} (ns)	Positive First Peak Current for 500 Ohm*, I_{pr} (A)	Current at 100 ns for 500 Ohm*, I_{100} (A)
100	1.5 - 2.0	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable
200	3.0 - 4.0	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable
400	6.0 - 8.1	67% to 90% of I_{ps1}	66 - 90	0.85 to 1.2	0.29 $\pm$10%
800	11.9 - 16.1	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable

* The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.

2.5 Automated ESD Test Equipment Relay Verification

If using automated ESD test equipment, the system diagnostics test shall be performed on all high voltage relays per the equipment manufacturer's instructions. This test normally measures continuity and will identify any open or shorted relays in the test equipment. Relay verification must be performed during initial equipment qualification and on a weekly basis. If the diagnostics test detects relays as failing, all sockets boards using those failed relays shall not be used until the failing relays have been replaced. The test equipment shall be repaired and requalified per section 2.3.

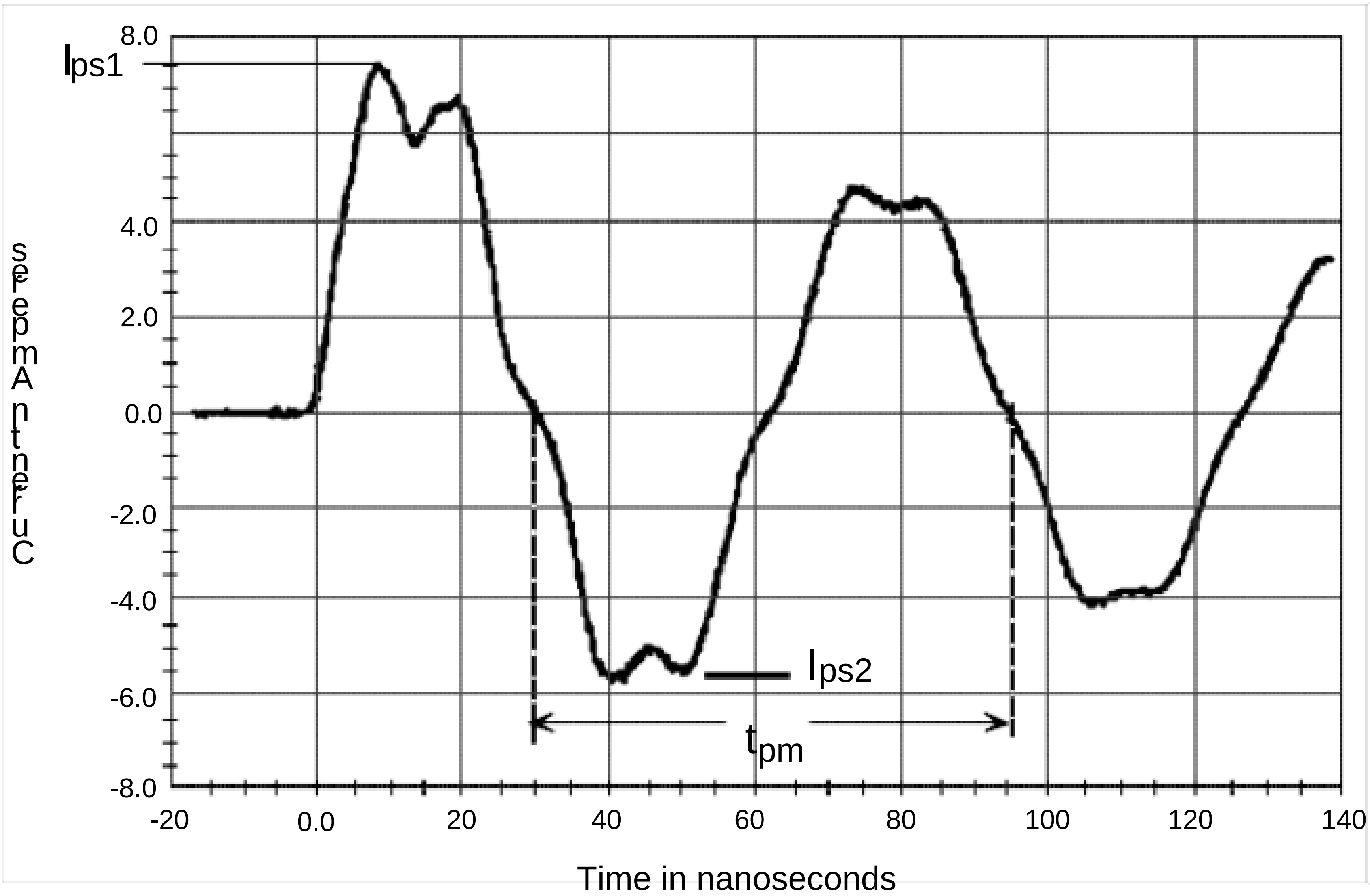

Figure 2: MM current waveform through a shorting wire, 400 volt discharge

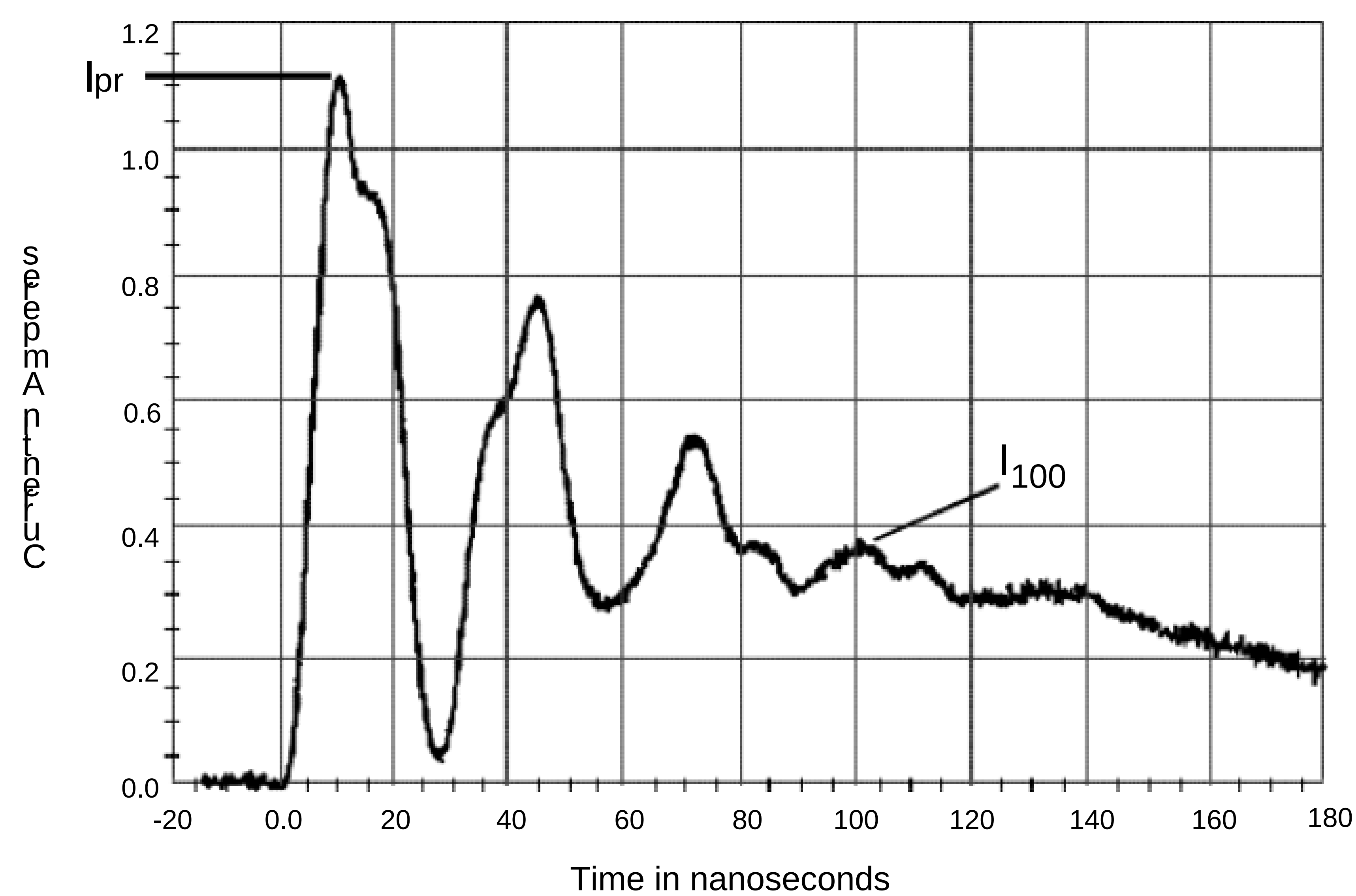

Figure 3: MM Current waveform through a 500 ohm resistor *, 400 volt discharge

* The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.

3. PROCEDURE

3.1 Sample Size

Each sample group shall be composed of three (3) units. Each sample group shall be stressed at one (1) voltage level using all pin combinations specified in Table 2. The use of a new sample group for each pin combination specified in Table 2 is also acceptable. Voltage level skipping is not allowed. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level. Therefore the minimum number of devices required for ESD qualification is 3 devices, while the maximum number of devices depends on the number of pin combinations and the number of voltage steps required to achieve the maximum withstanding voltage. For example, a device (1 VCC pin, 1 GND pin, and 2 IO pins) with a maximum withstanding voltage of 200 volts requires 4 voltage steps of 50 volts each, 3 pin combinations, and 3 devices per pin combination per voltage level for a maximum total of 36 devices.

Maximum # of devices = (# of pin combinations) X (# of voltage steps required) X 3 devices

3.2 Pin Combinations

The pin combinations to be used are given in Table 2. The actual number of pin combinations depends on the number of power pin groups. Power pins of the same name (VCC1, VCC2, VSS1, VSS2, etc.) may be tied together and considered one (1) power pin group if they are connected in the package or on the chip via a metal line. Same name power pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other, must be treated as a separate power pin group. All pins configured as "no connect" pins shall be considered non-supply pins and included in the pin groups stressed during ESD testing. Integrated Circuits with six (6) pins or less shall be tested using all possible pin pair combinations (one pin connected to terminal A, another pin connected to terminal B) regardless of pin name or function.

Table 2: Pin Combinations for Integrated Circuits

Pin Combination	Connect Individually to Terminal A (Stress)	Connect Individually to Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	First power pin(s)	All pins except PUT and first power pin(s)
2	All pins one at a time, except the pin(s) connected to Terminal B	Second power pin(s)	All pins except PUT and second power pin(s)
3	All pins one at a time, except the pin(s) connected to Terminal B	Nth power pin(s)	All pins except PUT and Nth power pin(s)
4	Each Non-supply pin	All other Non-supply pins except PUT	All power pins

3.3 Test Temperature

Each device shall be subjected to ESD pulses at room temperature.

3.4 Measurements

Prior to ESD testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed on all sample groups and all devices in each sample group per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.5 Detailed Procedure

The ESD testing procedure shall be per the test flow diagram of Figure 4 and as follows:

a. Set the pulse voltage at 50 volts. Voltage level skipping is not allowed.

b. Connect a power pin group to terminal B. Leave all other power pins unconnected (see Table 2 / pin combination 1).

c. Connect an individual pin to terminal A. Leave all other pins unconnected.

d. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

e. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

f. Disconnect the PUT from testing and connect the next individual pin to terminal A. Leave all other pins unconnected.

g. Repeat steps (d) through (f) until every pin not connected to terminal B is pulsed at the specified voltage.

h. Repeat steps (b) through (g) until all power pin groups have been stressed (see Table 2 / pin combinations 2 and 3). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

i. Connect one non-supply pin to terminal A and tie all other non-supply pins to terminal B. Leave all power pins unconnected (see Table 2 / pin combination 4). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

j. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

k. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

l. Disconnect the PUT from testing and connect the next non-supply pin to terminal A. Tie all non-supply pins not under test to terminal B. Leave all other pins unconnected (see Table 2 / pin combination 4).

m. Repeat steps (j) through (l) until all non-supply pins have been tested.

n. Test the next device in the sample group and repeat steps (b) through (m) until all devices in the sample group have been tested at the specified voltage level.

o. Submit the device for complete DC parametric and functional testing (final ATE verification) per the device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification, and determine whether the devices pass the failure criteria requirements specified in section 4. The functionality of "E^2PROM" type devices shall be verified by programming random patterns. If a different sample group is tested for each pin combination or stress voltage level, it is permitted to perform the DC parametric and functional testing (final ATE verification) per device specification after all sample groups have been tested.

p. Using the next sample group, increase the pulse voltage by 50 volts and repeat steps (b) through (o). Voltage level skipping is not allowed. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group pass the failure criteria requirements specified in section 4 after exposure to a specified voltage level.

q. Repeat steps (b) through (p) until failure occurs or the device fails to meet the 50V stress voltage level.

4. FAILURE CRITERIA

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5. ACCEPTANCE CRITERIA

A device passes a voltage level if all devices in the sample group stressed at that voltage level and below pass. All the devices and sample groups used must pass the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 3, the supplier shall classify the device according to the maximum withstanding voltage level.

Table 3: Integrated Circuit MM ESD Classification Levels

Component Classification	Maximum Withstand Voltage
M0	≤50 V
M1	> 50 V to ≤100 V
M2	> 100 V to ≤200 V
M3	> 200 V to ≤400 V
M4	> 400 V

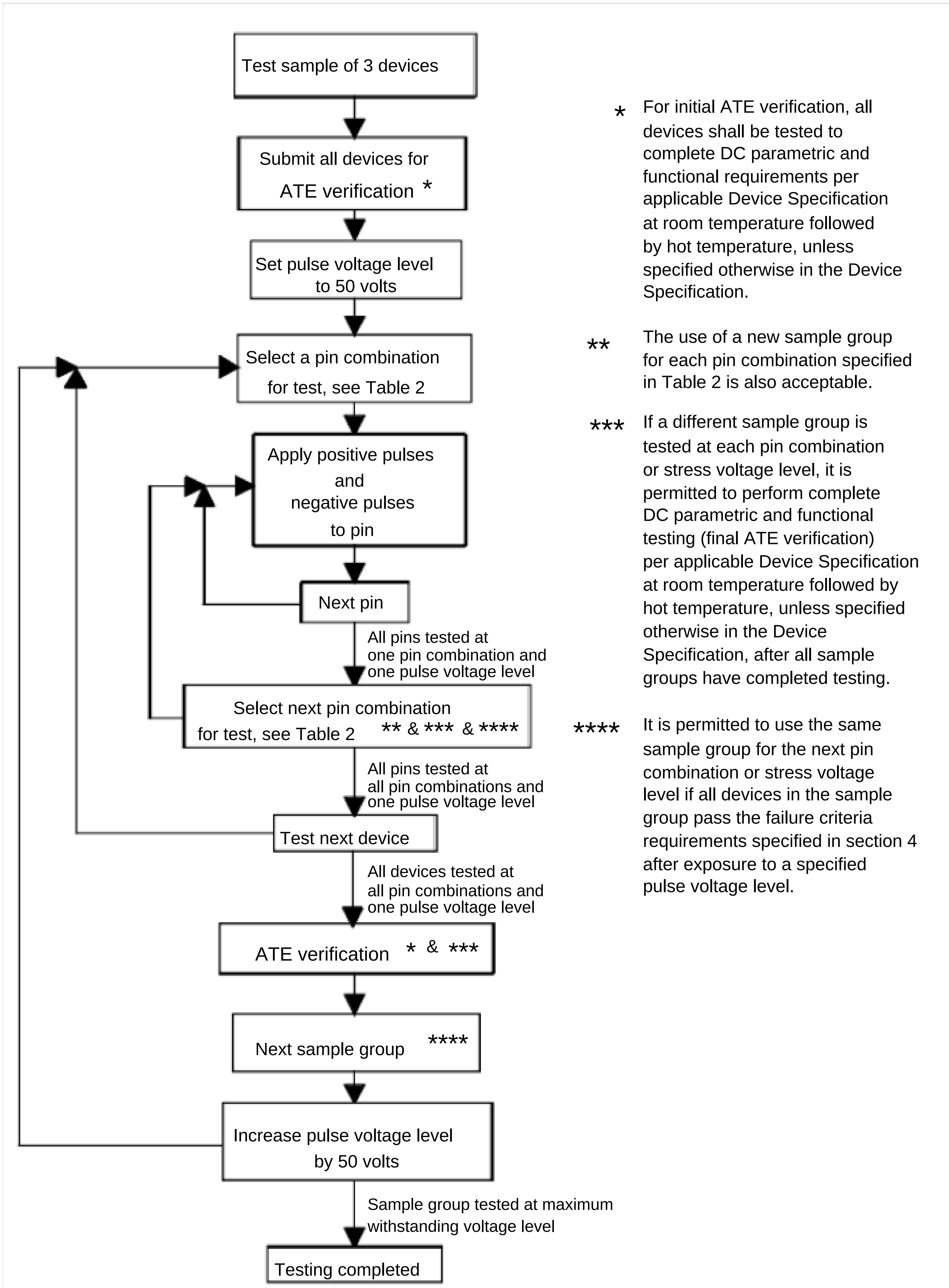

Figure 4: Integrated Circuit MM ESD Test Flow Diagram

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 15, 1995	Added Copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, I, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.
B	Sept. 6, 1996	Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.4.1 (d and f), 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Table 1; Figures 1 and 4.
C	Oct. 8, 1998	Revised the following: Sections 1.2, 2.1, 3.1, 3.5 (a and p); Tables 1 and 2; Figures 1 and 4. Revision to section 3.5 (a and p) and Figure 4 reflects a change from 100 volt increments to 50 volt increments. Revision to Table 1 reflects the addition of a 100 volt level and a ±15% tolerance applied to all Ips1 (positive first peak current for short) parameter values.
D	Aug. 25, 2000	Added note to page 1 concerning optional use of Q100-011 Field Induced Charged Device Model (FCDM) instead of Q100-003 Machine Model.
E	July 18, 2003	Revision to section 5 reflects addition of classification levels for ESD testing. New Table 3 added listing MM ESD classification levels.